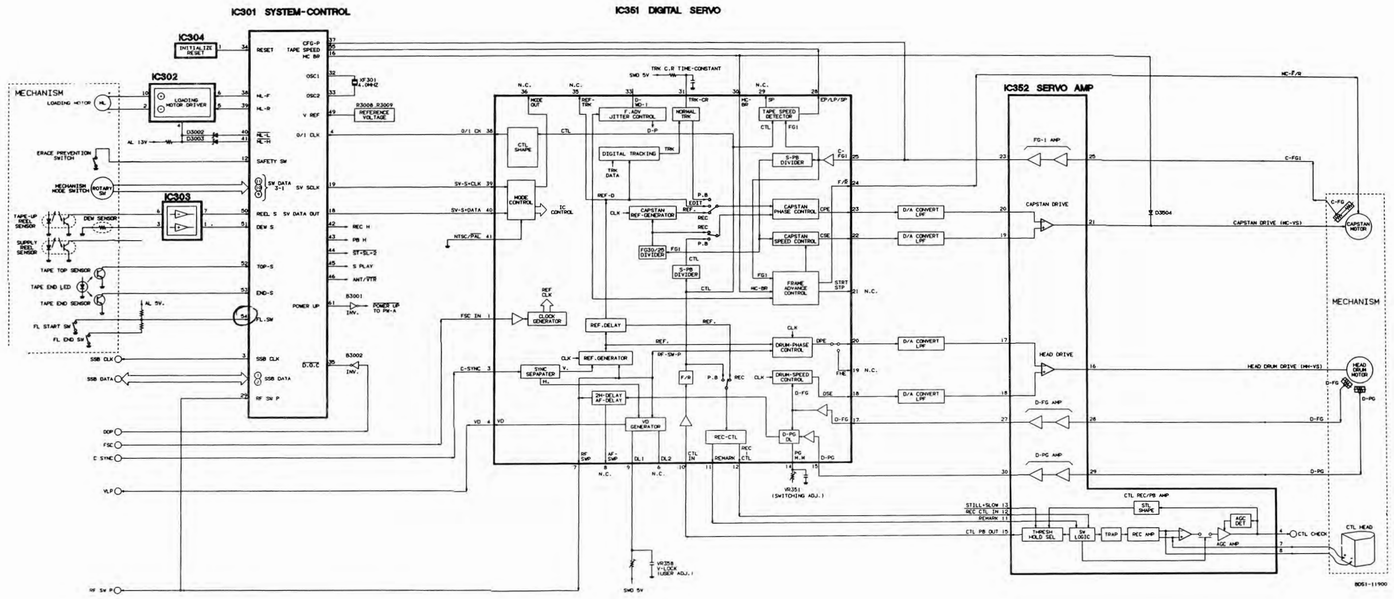
SYSTEM CONTROL & SERVO CIRCUIT BASIC BLOCK DIAGRAM



IC711 (M50957) TIMER MPU PIN FUNCTIONS TABLE

Pin No.	Port	Input/Output Signal	I/O	Input/Output Function
1	Vcc			+ 5V
2	P6₅	AV	O	"H" output when an external input is received.
3	P6₄	SC	O	"H" during simulcast.
4	P6₃/PWM3	BAND1	O	Band data output (BAND1, BAND2)
5	P6₂/PWM2	BAND2	O	(L, L) = VHF-LOW (L, H) = VHF-HIGH (H, L) = UHF (H, H) = SKIP
6	P6₁/PWM1	PWM	O	Tuning voltage output.
7	P6₀/T	ADJUST	O	Pulse output (6.29MHz/128) for clock frequency adjustment.
8	P2₇	$\overline{CLK}$	O	Clock pulse output to the E² PROM.
9	P2₆	DI	I/O	Data exchange with the E² PROM.
10	P2₅	$\overline{E^2 PROM\ CS1}$	O	E² PROM 1 is accessed when "L".
11	P2₄	BG/$\overline{L}$	O	Transmission system switching ("H" = PAL BG ; "L" = SECAM L).
12	P2₃	NC		NC
13	P2₂	TUNER ON	O	"H" output when tuner power is ON.
14	P2₁	$\overline{AUDIO\ MUTE}$	O	"L" output during AUDIO MUTE.
15	P2₀	AFT MUTE	O	"H" output during AFT MUTE.
16	P3₇/$\overline{Srdy}$	$\overline{POWER\ DOWN}$	O	Power failure mode set at "L" input.
17	P3₆/CLK	$\overline{SCLK}$	I	SSB clock pulse input.
18	P3₅/Sout	$\overline{SOUT}$	O	SSB data output.
19	P3₄/Sin	SIN	I	SSB data input.
20	P3₃/ANin	AFT.C	I	AFT.S curve input.
21	P3₂/CNTR	H.SYNC	I	Horizontal sync signal input for existence channel discrimination.
22	P3₁	SCL	O	Clock pulse output to the VPS decoder IC.
23	P3₀	SDA	I/O	Data exchange with the VPS decoder IC.
24	P5₃/INT1	V. SYNC	I	Vertical sync signal input for existence channel discrimination.
25	P5₂/INT2	REMOCON	I	Remote control signal input.
26	CNVss			Ground.
27	$\overline{RESET}$			Reset terminal.
28	Xin			8.291456MHz clock terminal.
29	Xout			
30	Xcin			32.768kHz (clock OSC used in the power failure mode)
31	Xcout			
32	Vss			Ground
33	ϕ			
34	P5₇	KEY IN4	I	Key inputs
35	P5₆	KEY IN3	I	
36	P5₅	KEY IN2	I	
37	P5₄	KEY IN1	I	
38	Vp	Vp		-30V
39	P5₁	NC	—	NC
40	P5₀	NC	—	NC
41	P1₇	o	O	Display segment outputs. (Included key-scan output)
42	P1₆	n	O	
43	P1₅	m	O	
44	P1₄	l	O	
45	P1₃	k	O	
46	P1₂	j	O	
47	P1₁	i	O	
48	P1₀	C9	O	Display grid outputs.
49	P0₇	C8	O	
50	P0₆	C7	O	
51	P0₅	C6	O	
52	P0₄	C5	O	
53	P0₃	C4	O	
54	P0₂	C3	O	
55	P0₁	C2	O	
56	P0₀	C1	O	
57	P4₇	h	O	Display segment outputs. (Included key-scan output)
58	P4₆	g	O	
59	P4₅	f	O	
60	P4₄	e	O	
61	P4₃	d	O	
62	P4₂	c	O	
63	P4₁	b	O	
64	P4₀	a	O	

IC301 (LC66508B) SYSTEM CONTROL MPU PIN FUNCTIONS TABLE

Pin No.	Input/Output Signal	I/O		Input/Output Function
1	SSB DATA	I/O	SSB	SSB input/output data
2				
3	SSB CLK	O		Clock pulse output to SSB.
4	0/1 CLK	I	External interrupt	CTL signal input for realtime counter.
5	REF 254	I		30Hz pulse. Synchronized to VIDEO in the EE mode, and to the RF switch pulse during playback.
6	———	—		
7	———	—		
8				+ 5V
9	SW DATA 1	I	Mechanism switch	Switches showing the mechanism position.
10	SW DATA 2	I		
11	SW DATA 3	I		
12	E. P SW	I		Switch for determining whether cassette recording is possible.
13	—	—		
14	PAL	I	Servo	PAL/NTSC system input. "L" is for PAL.
15	CTL GAIN DOWN	O		CTL AMP circuit gain switching signal. Output at POS SW 2 and less.
16	MC-BR	O		Capstan motor brake signal.
17	———	—	Serial servo data	
18	SV S.DATA	O		Serial data output to the servo IC.
19	SV S.CLK	O		Serial clock pulse output to the servo IC.
20	———	—	———	
21	———	—		
22	———	—		
23	———	—		
24	———	—		
25	———	—		
26	———	—		
27	———	—		
28	———	—		
29	RF SW P.	I	External	0 to 30Hz pulse. 30Hz during playback, etc.
30	TEST		Ground	
31	Vss			
32	OSC1		MPU clock oscillation output pins. Clock frequency is 4MHz.	
33	OSC2			
34	RESET	I		MPU initial setting or all-clear.
35	DOC P.	I	External interrupt	* Pulse with an amplitude greater than 0 and smaller than 33ms. STILL noise shifting pulse (output in the STILL mode).
36	SP/LP	I		Tape speed selection command signal input.
37	C. FG P.	I		0 to approx. 6kHz pulse. The frequency required for recognition is approx. 300Hz.
38	ML-F	O	Motor drive	Forward direction loading command signal (FL, TL).
39	ML-R	O		Reverse direction loading command signal (FL, TL).
40	ML-L	O		Low loading speed command signal.
41	ML-M	O		Medium loading speed command signal.
42	REC H	O	Video	Recording command signal.
43	P. B. HIGH	O		Playback screen output command signal.
44	STILL+SLOW+X2S	O		(Output in the STILL, SLOW and X2S modes).
45	SPECIAL PLAY	O		Output in the special playback (CUE, REV, STILL, SLOW, F.ADV, A. DUB PAUSE) modes.
46	ANT/VIDEO	O		ANT/VIDEO switching signal.
47	———	—		
48	———	—		
49	REF VOLT	I	Sensor	Reference voltage for the microcomputer built-in comparator.
50	REEL P.	I		0 to approx. 300Hz pulse. Its period changes according to reel table rotation.
51	DEW S.	I		For dew detection.
52	TAPE TOP S.	I		For tape winding start detection.
53	TAPE END S.	I		For tape winding end detection.
54	FL SW	I	Mechanism switch	Front loading mechanism' switch (3 values input : Low = cassette out ; medium = FL mode ; high = cassette loading completed).
55	TAPE SPEED	I	Servo	Result of tape speed detection by the servo system (high = LP ; low = SP).
56	A・MUTE	O	Audio	Audio output inhibiting indication signal.
57	A・REC MUTE	O		Normal audio output and recording inhibiting indication signal.
58	———	—		
59	———	—		
60	———	—		
61	POWER UP	O	Power supply	Output always except when power is off.
62	———	—		
63	CAP. M	I	Option	For kind of Capstan motor detection.
64	Vcc			+ 5V

IC351 (LC7416) DIGITAL SERVO IC PIN FUNCTIONS TABLE

Pin No.	I/O Terminal Name	I/O	Input/Output Function
1	FSC IN	I	Input for the IC internal system clock pulse. A level of at least 0.3 V_{P-P} is required. The color subcarrier signal is input by capacitive coupling.
2	Vss		Ground
3	C-SYNC	I	Composite sync signal input.
4	VD	O	Dummy V_D signal output.
5	NC	—	NC
6	NC	—	
7	RF-SW-PULSE	O	Video head switching pulse output.
8	AF-SW-PULSE	O	Audio head (FM) switching pulse output.
9	DL1	I	Dummy V_D insertion position control CR.
10	CTL-IN	I	Control signal input.
11	REMAK	O	Outputs the control signal re-recording control signal, Three-value output (H, M, L).
12	REC-CTL	O	Recording control signal output. Three-value output (H, OPEN, L).
13	NC	—	NC
14	D-PG. MM	I	CR for drum .PG signal delay.
15	D-PG	I	Drum PG signal input.
16	NC	—	NC
17	D-FG	I	Drum FG signal input.
18	DSE	O	Outputs the speed error for drum system speed control. An output making the drum motor stop is delivered when DRUM-ON is "0". The lower three bits of the output data forms R-2R ladder network and the 4th bits for DAC (D/A Converter) and upper 5th to 8th bits for PWM (Pulse Width Modulation).
19	FHE	O	Outputs the horizontal sync signal of the composite sync signal after F-V conversion (using the drum phase control system). The lower three bits of the output data forms R-2R ladder network and the 4th bits for DAC (D/A Converter) and upper 5th to 8th bits for PWM (Pulse Width Modulation).
20	DPE		Error output for drum system phase control. The lower three bits of the output data forms R-2R ladder network and the 4th bits for DAC (D/A Converter) and upper 5th to 8th bits for PWM (Pulse Width Modulation).
21	C-START/STP	O	Outputs the capstan motor start and brake pulses in the slow mode.
22	CSE	O	Capstan system speed error output. An output making the capstan motor stop is delivered when CAP-ON is "0". The lower three bits of the output data forms R-2R ladder network and the 4th bits for DAC (D/A Converter) and upper 5th to 8th bits for PWM (Pulse Width Modulation).
23	CPE	O	Capstan system phase reciprocal error output. The lower three bits of the output data forms R-2R ladder network and the 4th bits for DAC (D/A Converter) and upper 5th to 8th bits for PWM (Pulse Width Modulation).
24	F/R	O	Capstan motor forward/reverse control output. "1" sets the reverse mode, and "0" the forward mode.
25	C-FG1	I	Capstan FG signal input.
26	NC	—	NC
27	NC	—	NC
28	EP/LP/SP	O	Recording mode output. Three-value output ("H" is for EP mode, "M" for LP mode and "L" for SP mode).
29	SP	O	Recording mode output. "H" is for SP mode.
30	CAP-BRK	I	Control input for capstan brake timing. (MC-BR)
31	TRK-CR	I	CR for tracking adjustment.
32	NC	—	NC
33	D-WD1	I	CR for drum compensation timing adjustment in the slow mode.
34	NC	—	NC
35	REF-TRK	O	Outputs the tracking delay input signal.
36	MODE (×2+STILL)	O	Mode decoding signal output. At the ×2 SPEED mode and starting time of SLOW/STILL mode, output "H" level.
37	NC	—	NC
38	1/0-CK	O	Outputs the CTL signal for realtime counter.
39	SV-S・CLK	I	Serial transmission clock pulse input.
40	SV-S・DATA	I	Serial data input terminal.
41	NTSC/PAL	I	NTSC/PAL switching input. "H" is for NTSC, "L" for PAL.
42	V_{DD}		+ 5V supply terminal

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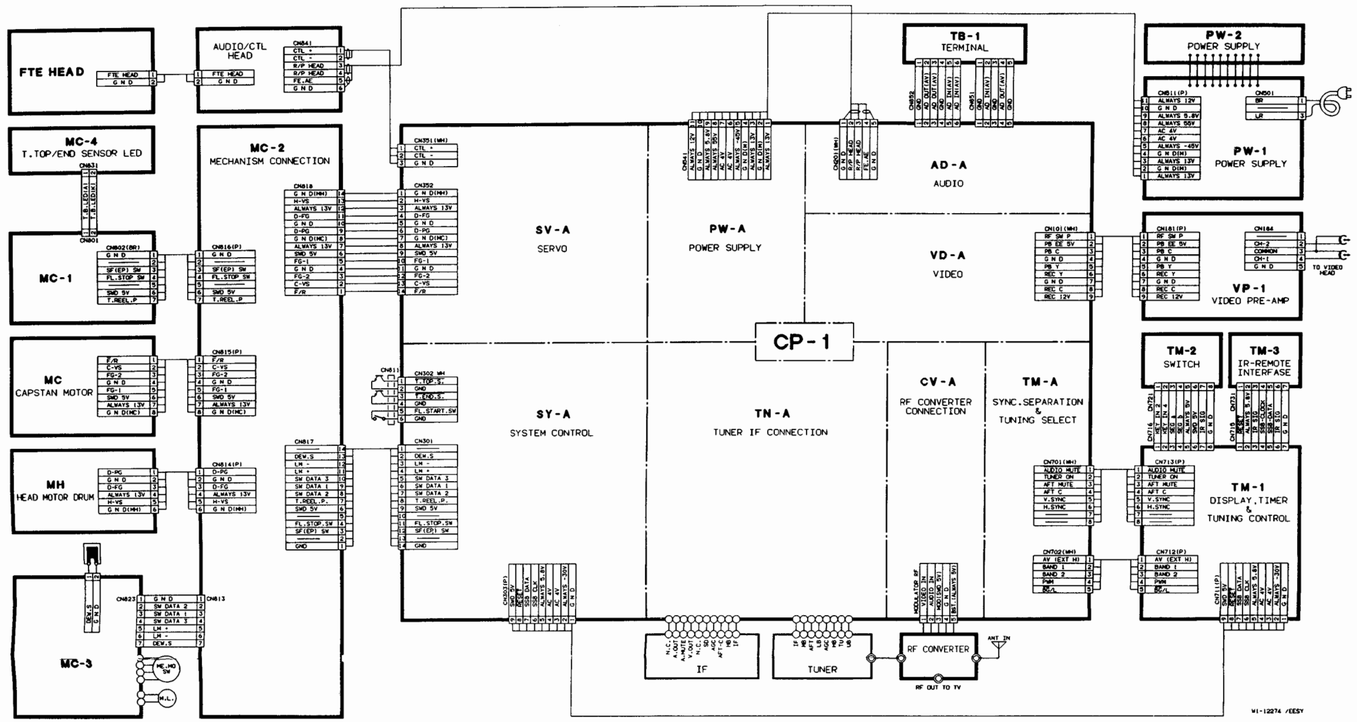
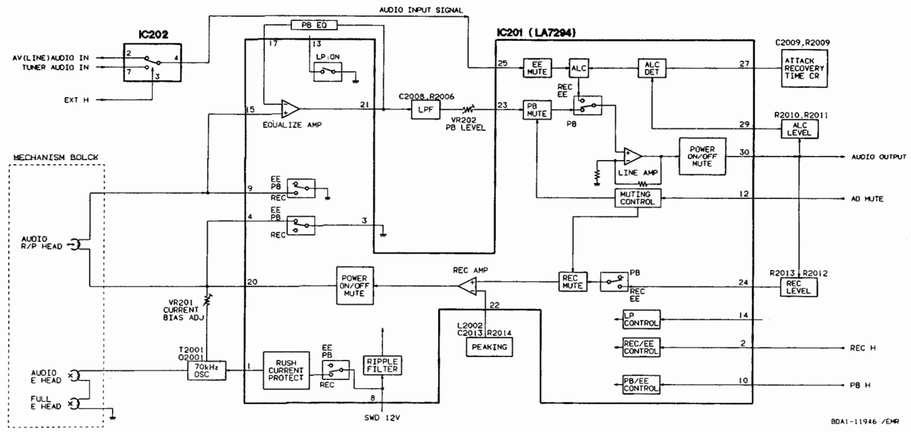
1AC6P22A02500 KP1/EE-SY (0989SY01)

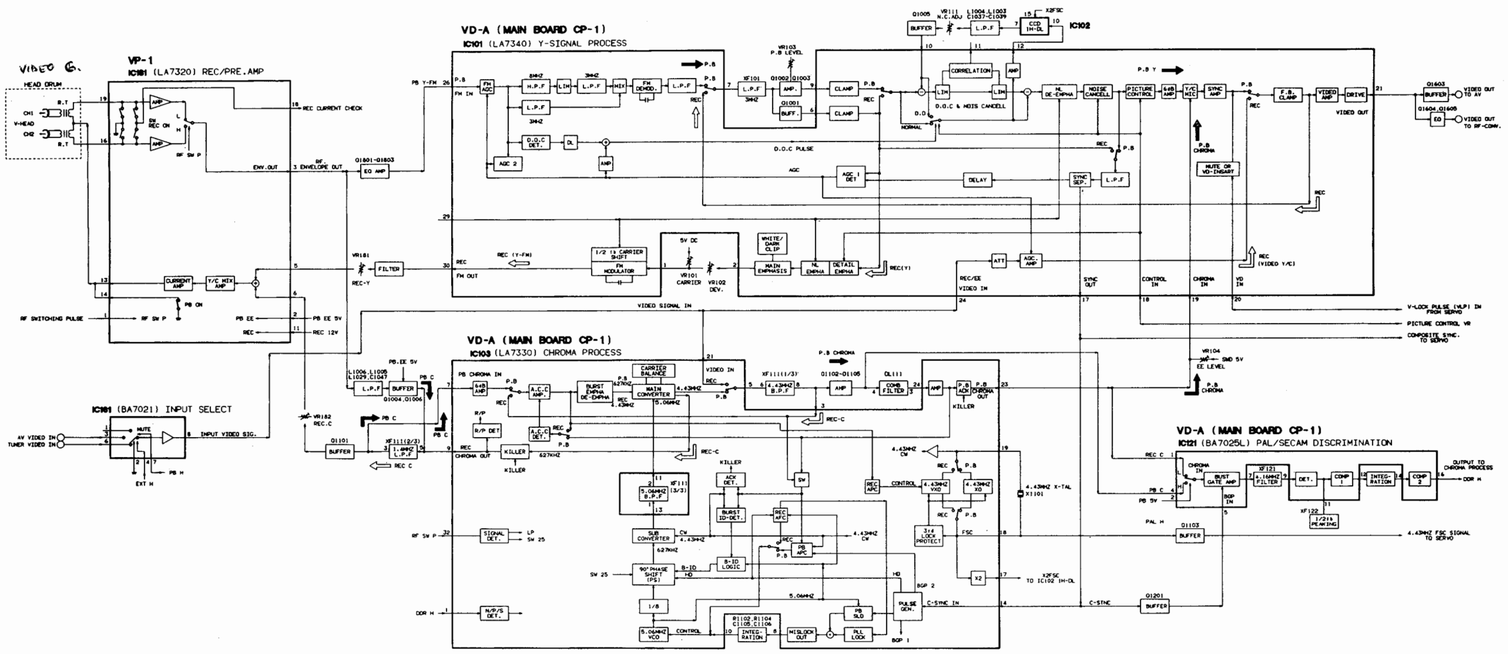
OVERALL WIRING DIAGRAM



AUDIO CIRCUIT BASIC BLOCK DIAGRAM



VIDEO CIRCUIT BASIC BLOCK DIAGRAM



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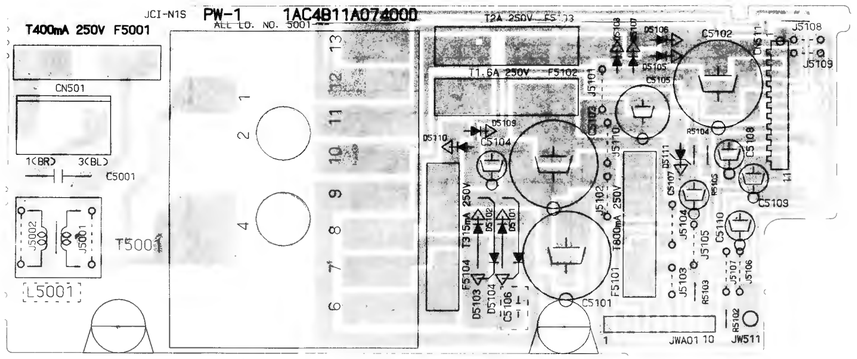
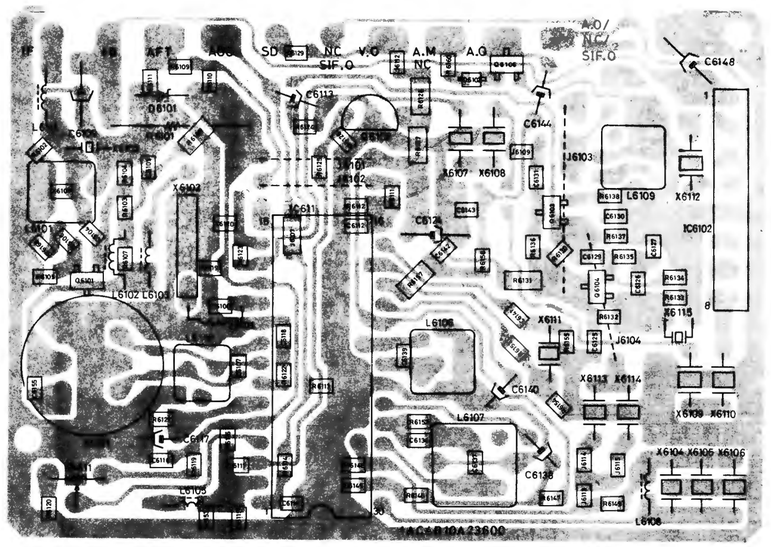
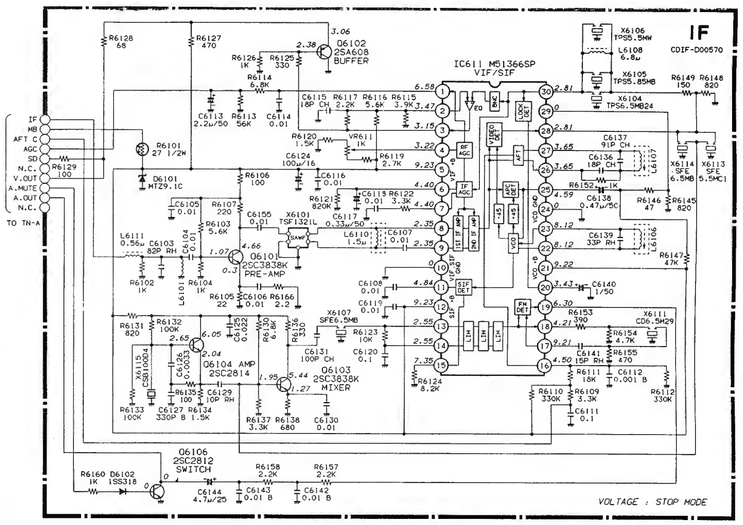
PW-1 (POWER SUPPLY) PRINTED WIRING BOARD



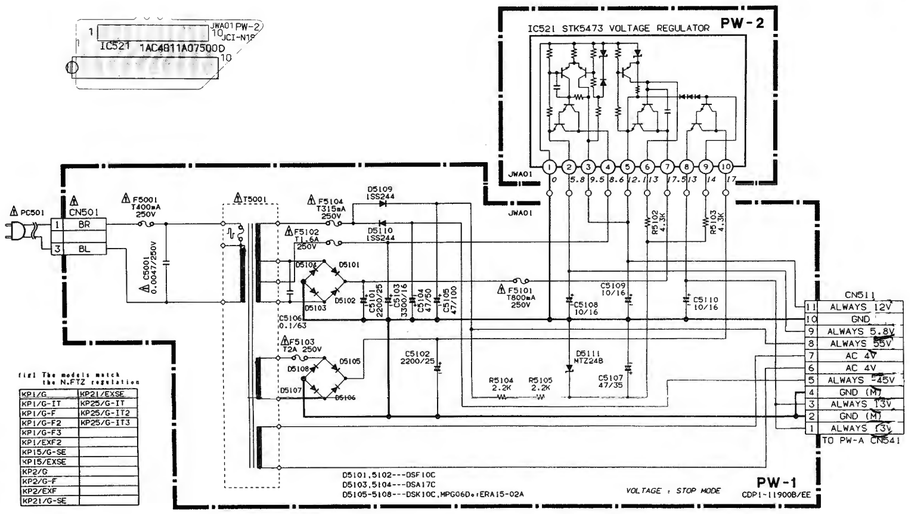
IF PRINTED WIRING BOARD



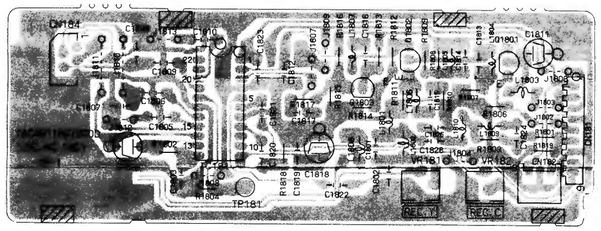
IF SCHEMATIC DIAGRAM



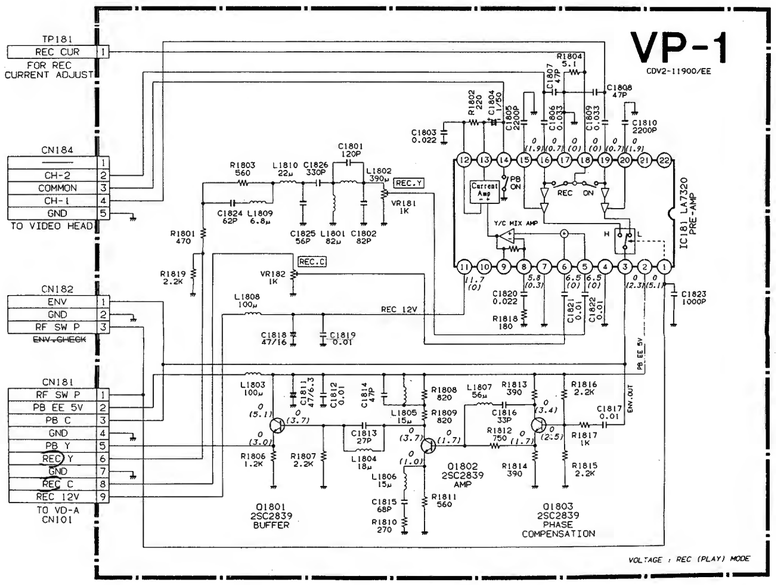
PW-1, PW-2 (POWER SUPPLY) SCHEMATIC DIAGRAM



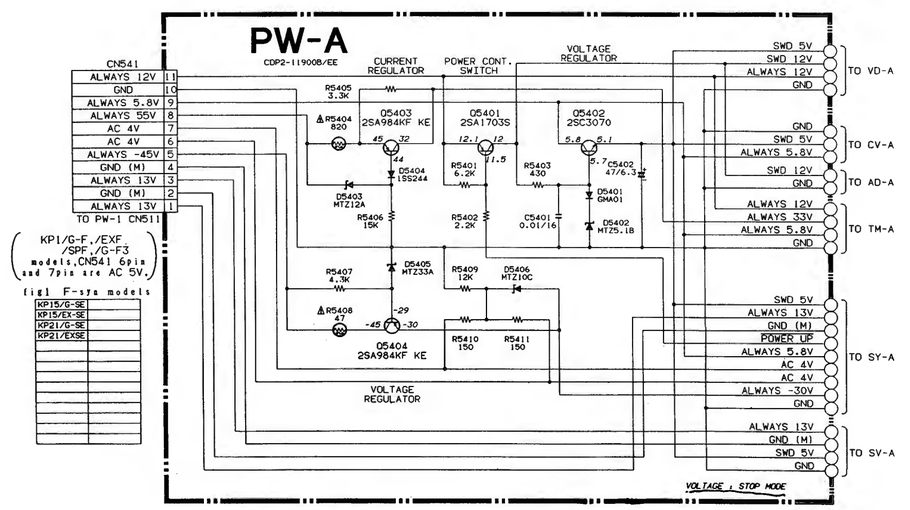
VP-1 (VIDEO PRE-AMP) PRINTED WIRING BOARD



VP-1 (VIDEO PRE-AMP) SCHEMATIC DIAGRAM

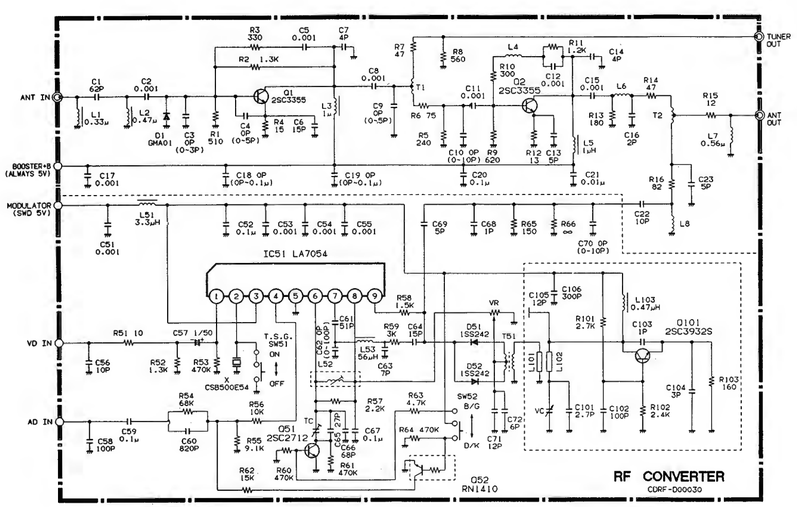


COMPL. CP-1 (PW-A) (POWER SUPPLY) SCHEMATIC DIAGRAM



RF CONVERTER SCHEMATIC DIAGRAM

RF CONVERTER SCHEMATIC DIAGRAM



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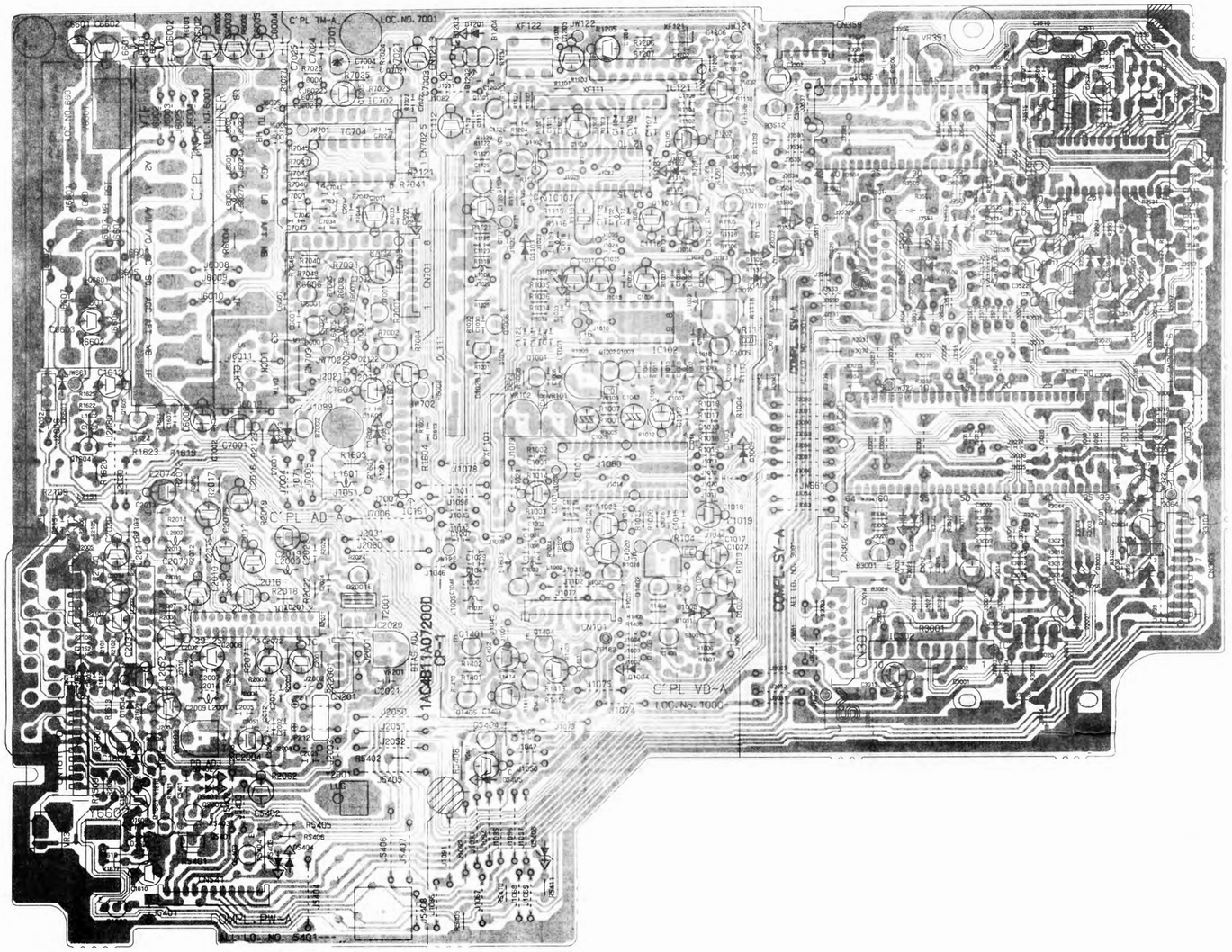
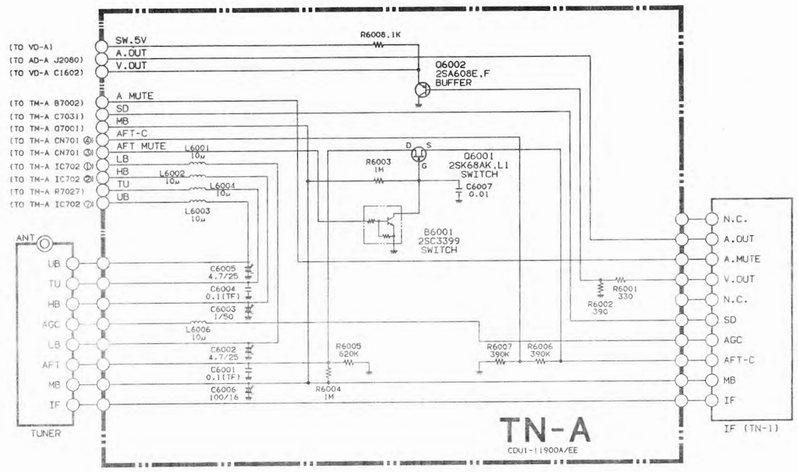
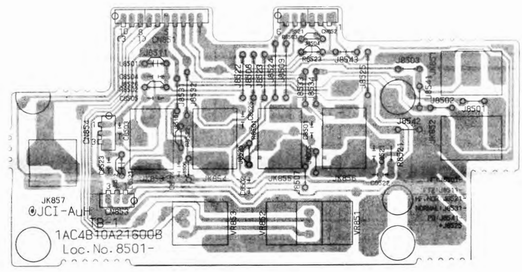
CP-I (MAIN) PRINTED WIRING BOARDS



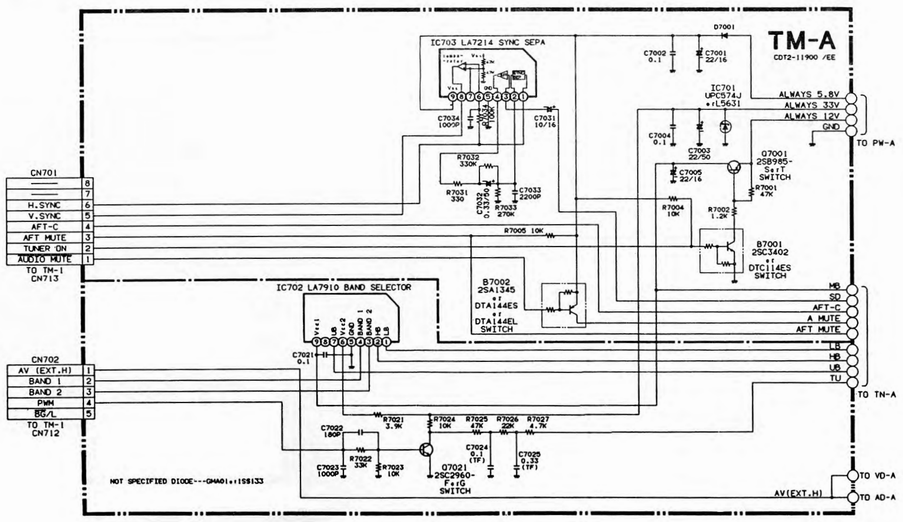
COMPL. CP-I (TN-A) (TUNER IF CONNECTION) SCHEMATIC DIAGRAM



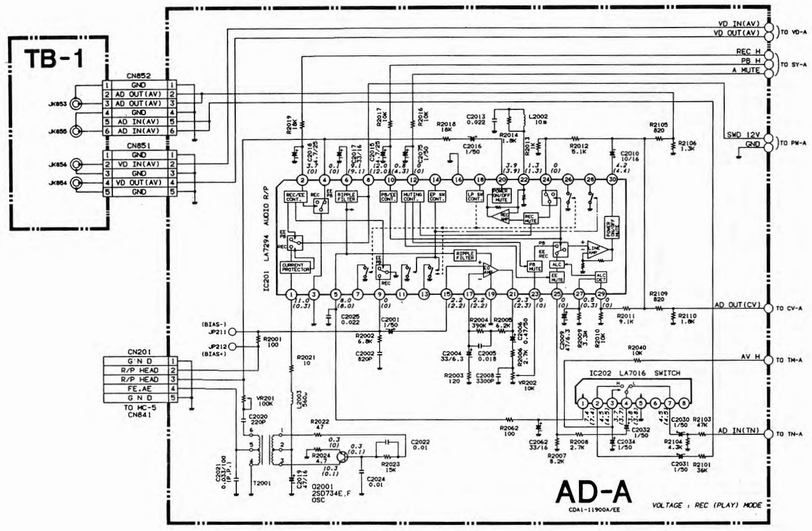
TB-1 (TERMINAL) PRINTED WIRING BOARD



COMPL. CP-I (TM-A) TIMER-2 SCHEMATIC DIAGRAM



COMPL. CP-I (AD-A) (AUDIO & COMPL.), TB-1 (TERMINAL) SCHEMATIC DIAGRAM



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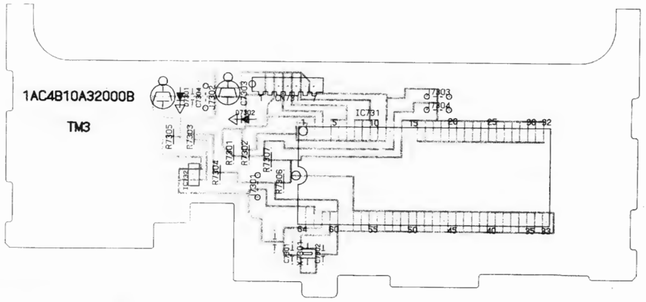
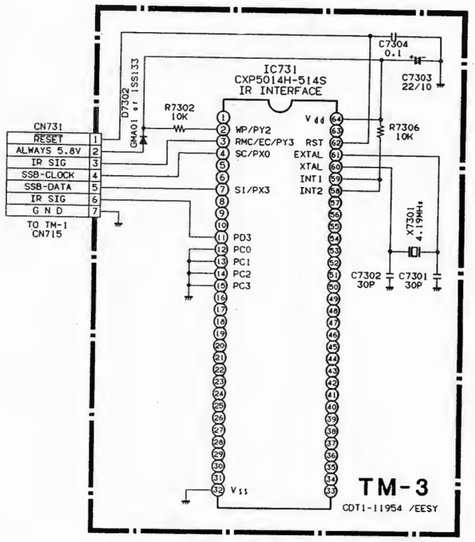
TM-3 (IR-REMOTE INTERFACE) PRINTED WIRING BOARD

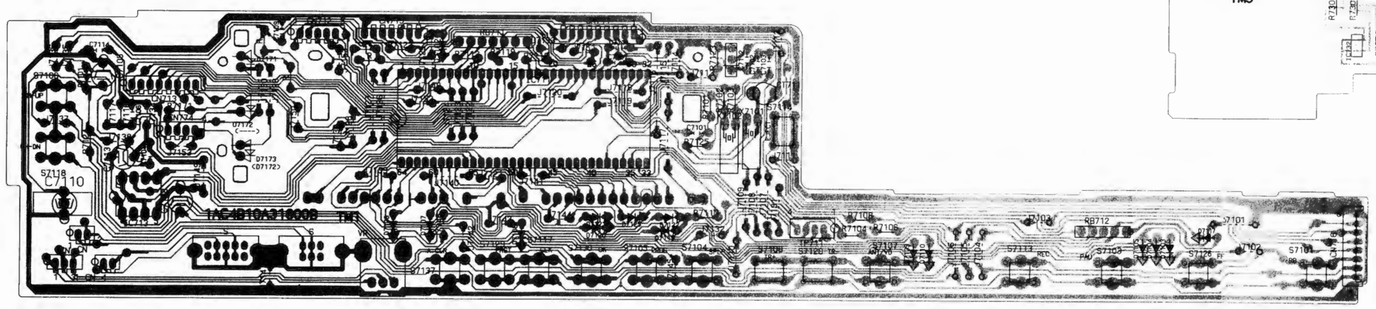


TM-3 (IR-REMOTE INTERFACE) SCHEMATIC DIAGRAM

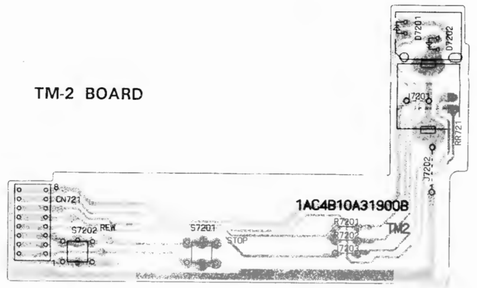


TM-1, TM-2 (CD TIMER-1) PRINTED WIRING BOARD

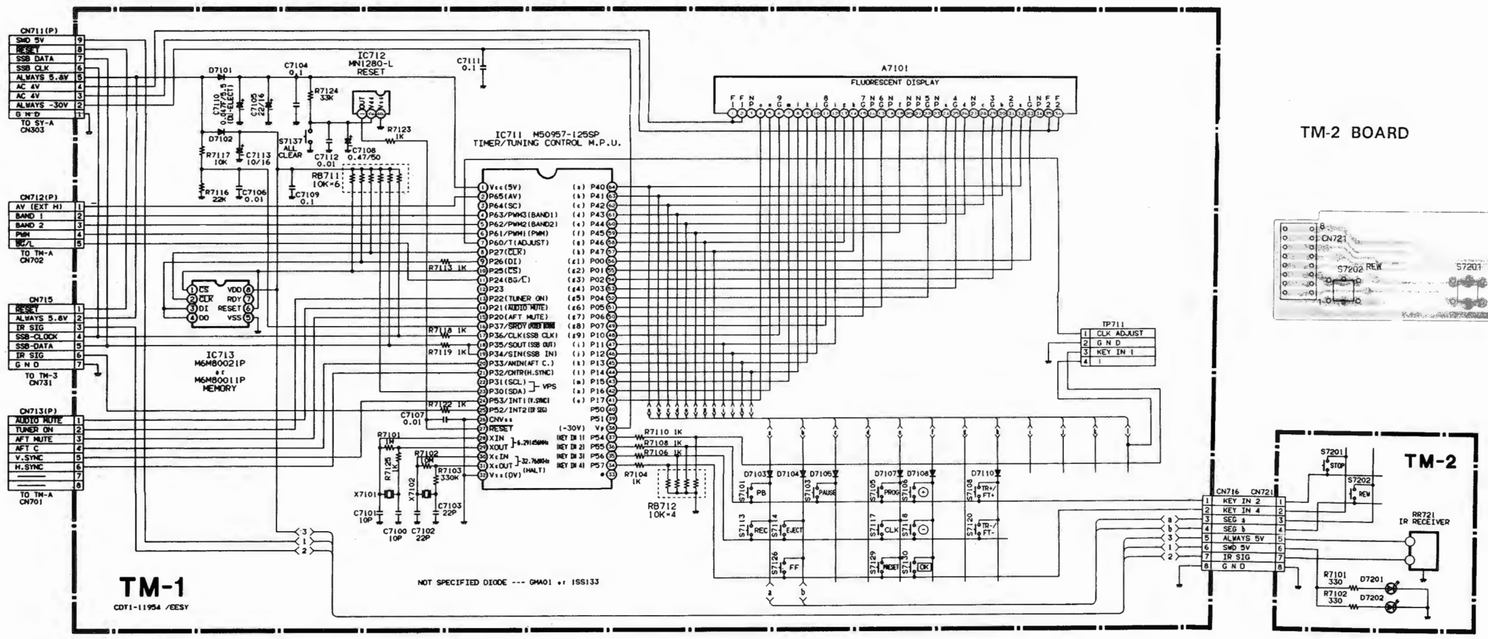
TM-1 BOARD



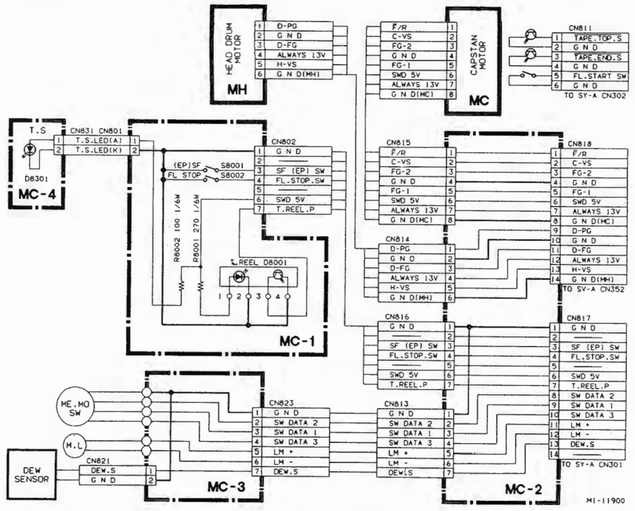
TM-2 BOARD



TM-1, TM-2 (CD TIMER-1) SCHEMATIC DIAGRAM



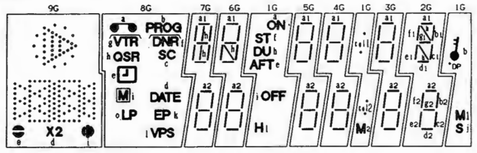
MECHANISM CONNECTION SCHEMATIC DIAGRAM



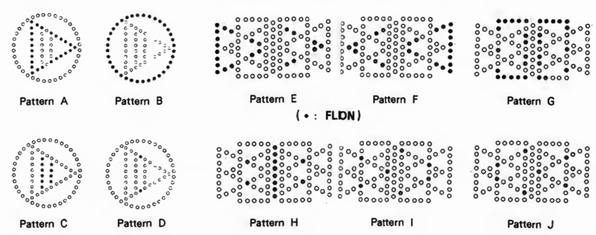
ANODE CONNECTION

	9G	8G	7G	6G	5G	4G	3G	2G	1G
a	B	●●	a1	a1	a1	a1	a1	a1	ON
b	A	PROG.	b1	b1	b1	b1	b1	b1	1
c	-	SC	c1	c1	c1	c1	c1	c1	DP
d	+2	DATE	d1	d1	d1	d1	d1	d1	M(1)
e	●	◪	e1	e1	e1	e1	e1	e1	AFT
f	C	DNR	f1	f1	f1	f1	f1	f1	ST
g	D	VTR	g1	g1	g1	g1	g1	g1	colon1
h	-	QSR	/	\	-	-	-	\	DU
i	●	H	a2	a2	a2	a2	a2	a2	OFF
j	E	-	b2	b2	b2	b2	b2	b2	S
k	I	EP	c2	c2	c2	c2	c2	c2	-
l	H	VPS	d2	d2	d2	d2	d2	d2	H
m	J	-	e2	e2	e2	e2	e2	e2	M(2)
n	F	-	f2	f2	f2	f2	f2	f2	-
o	G	LP	g2	g2	g2	g2	g2	g2	colon2

GRID ASSIGNMENT



9G : GRAPHIC MOE DISPLAY



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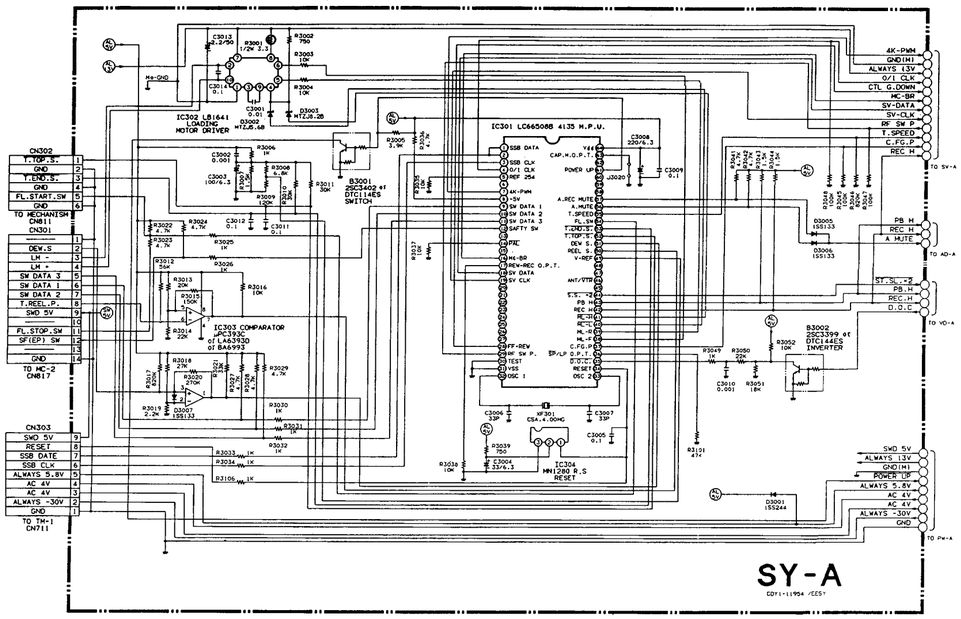
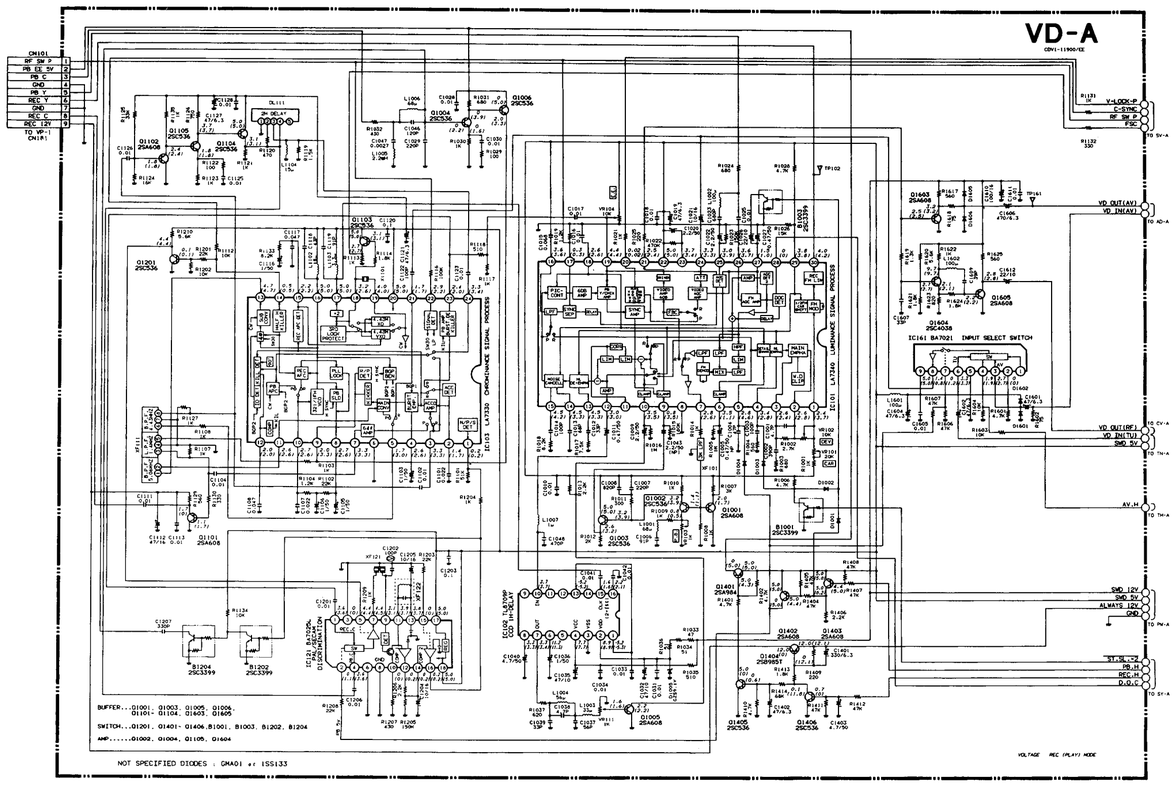
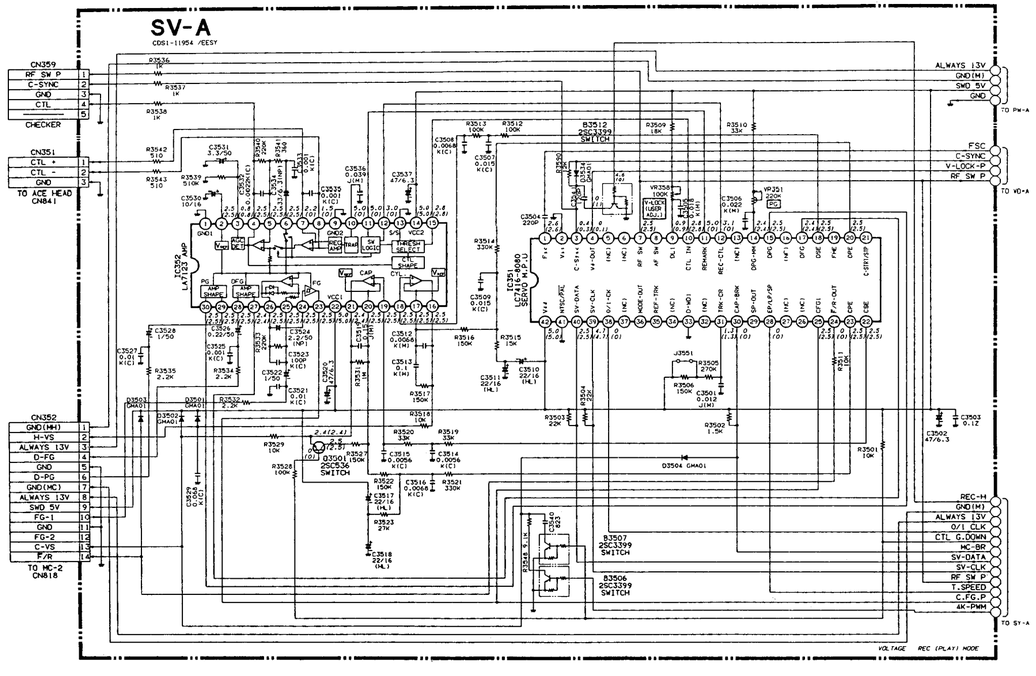
COMPL. CP-I (SY-A) (SYSTEM CONTROL) SCHEMATIC DIAGRAM



COMPL. CP-I (VD-A) (VIDEO) SCHEMATIC DIAGRAM



COMPL. CP-I (SV-A) (SERVO) SCHEMATIC DIAGRAM



WAVEFORM OF SERVO CIRCUIT

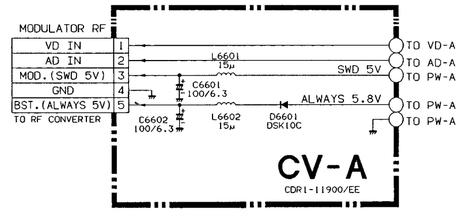
IC351 (LC7416)

⑦	4.9V, 20msec 20msec	㉕	4V, 2 msec = 504Hz
⑧	5V, 20msec 20msec	㉑	3V, 3 msec, 40 msec
⑨	3V, 0.4 msec, 20 msec	㉒	5V, 17 μsec, 40 msec
⑩	REC 3.8V, 24 msec 16 msec; P.B 3.9V, 24 msec 16 msec	①	1Vp-p, 4.43 MHz
⑫	REC 5V, 24 msec 16 msec	③	3.7V, T = 20 msec
⑭	3V, 2.1 msec, 20 msec	④	P.B 1.2 Vp-p
⑮	3.9V, 40 msec	⑦ ⑧	REC 3.2V, 24 msec 16 msec
⑰	4V, 1.33 msec = 750Hz	⑫	5V, 24 msec 16 msec
⑱ ⑳ ㉒ ㉓	5V, 8.593kHz		

IC352 (LA7123)

⑮	REC 3.8V, 24 msec 16 msec; P.B 3.9V, 24 msec 16 msec	㉓	4V, 2 msec = 504Hz
㉔ ㉖	1.2Vp-p, 2 msec = 504 Hz	㉗	4V, 1.33 msec = 750Hz
㉘	10 mVp-p, 1.33 msec	㉙	150 mVp-p, 40 msec
㉚	3.9V, 40 msec		

COMPL.CP-I (CV-A) (RF CONVERTER CONNECTION) SCHEMATIC DIAGRAM



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