HYUNDAI SEMICONDUCTOR

HY18CV8

CMOS EEPLD

L111202B-JAN92

DESCRIPTION

The HY18CV8 is a CMOS Electrically Erasable Programmable Logic Device (EEPLD) that provides a high performance; low power, reprogrammable and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the HY18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the HY18CV8 not only reduces development and field retrofit cost but enhances testability enabling HYUNDAI to ensure 100% field programmability and function. Packaged in a cost effective "window-less" 20 pin DIP, the flexible architecture of the HY18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20 pin bipolar PAL® devices and the Altera EP310/320. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Primary development and programming support of the HY18CV8 is provided by popular third-party PC based development tools and stand-alone programmers.

FEATURES

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - **CMOS : 20mA Standby +0.7mA/MHz max.**
  - **TTL : 25mA Standby +0.7mA/MHz max.**
- **High Performance**
  - **t_{PD} 25ns max., t_{CO} 18ns max., t_{SC} 20ns min.**
- **Reprogrammability**
  - **100% factory tested**
  - **Cost effective "window-less" package**
  - **3 second erase/program time**
  - **Adds convenience, reduces field retrofit and development cost**
- **Design Security**
  - **Prevents unauthorized reading or copying of design**
- **Architectural Flexibility**
  - **74 Product Term×36 Input Arrays**
  - **Up to 18 inputs and 8 I/O pins**
  - **Independently configurable I/O macro cell ; polarity, register, combinatorial, bi-directional**
  - **Synchronous preset, asynchronous clear**
  - **Independent output enables**
- **Application Versatility**
  - **Replaces SSI/MSI logic**
  - **Emulates bipolar PAL® devices and the Altera EP300/310**
  - **Replaces low density Gate Arrays**
  - **Simplifies inventory control**
  - **Allows new design possibilities**
- **Development/Programmer Support**
  - **Popular PC based development tools and programmers.**

BLOCK DIAGRAM

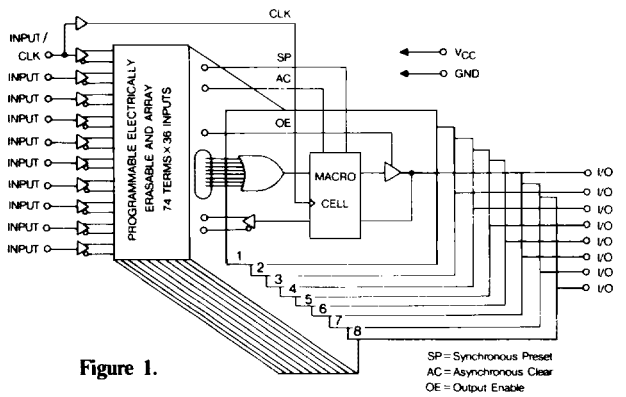
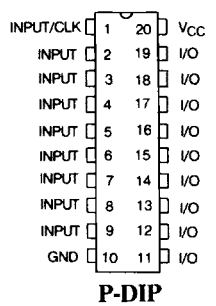


Figure 1.

PIN CONNECTIONS



P-DIP

PIN NAMES

INPUT/CLK	INPUT AND/OR CLOCK
INPUT	INPUT
I/O	BI-DIRECTIONAL INPUT/OUTPUT
V_{CC}	POWER SUPPLY(+5V)
GND	GROUND

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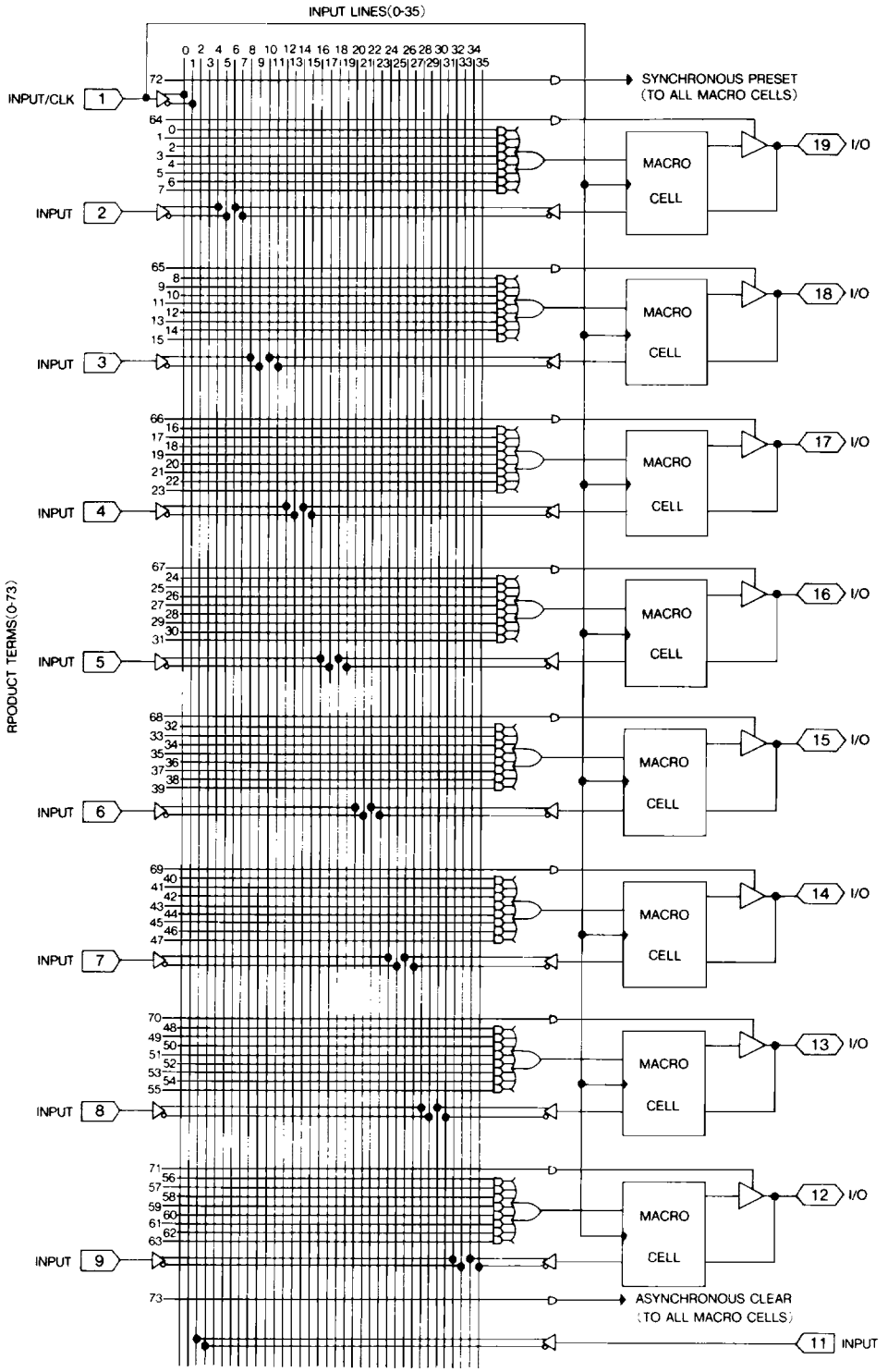
Figure 2. HY18CV8 Logic Array Diagram



ARCHITECTURAL OVERVIEW

The basic architecture of the HY18CV8 is similar to of earlier generation PLDs to the extent that utilizes a sum-of-products logic array in a programmable AND fixed OR structure. This familiar logic arrangement allows user defined output functions to be created by programming the connection of input signals into the array. What makes the architecture of the HY18CV8 different, however, is the increased capability and flexibility it provides in a higher level of equivalent gate integration and a simplification of design.

The block diagram in figure 1. illustrates the key elements of the HY18CV8 architecture. Externally, the HY18CV8 provides up to 18 inputs and 8 outputs for use. At the core is a programmable electrically erasable "AND array" of 36 input lines by 74 product terms. The 36 input lines are derived from the true and complement of the 18 possible input pins. The 74 product terms are made up of ; 1 synchronous preset term, 1 asynchronous clear term, 8 output enable terms and 64 terms divided into groups of 8 each feeding into an OR function.

Each OR function is directly associated with one of eight macro cells and I/O pins. An individual macro cell can be programmed into one of twelve different configurations. Depending on the configuration, the output of the macro cell can be fed back into the array or output via its associated I/O pin. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The output enable term of each I/O pin can be used to force a high impedance state for bidirectional I/O operations or for dedicated input usage. The synchronous preset term, asynchronous clear term and clock (pin 1. INPUT/CLK) are globally routed to all macro cells.

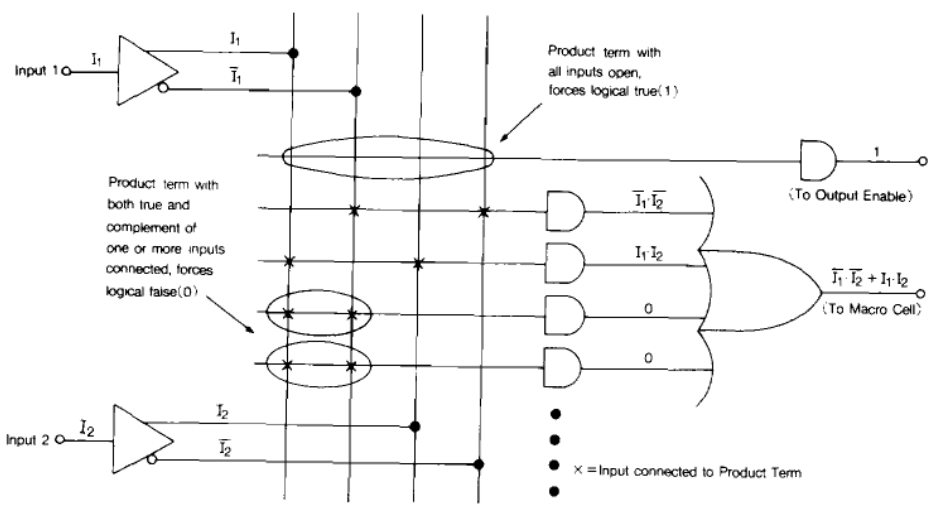
LOGIC ARRAY OPERATION

A more detailed view of the overall architecture, specifically the logic array, is illustrated by the HY18CV8 Logic Array Diagram in figure 2. As referred to previously, the logic array of the HY18CV8 consists of ;

36 Input Lines :
- 10 true and complement inputs
- 8 true and complement inputs/feedbacks

74 Product Terms :
- 64 product terms (8×8 Sum-of-Products terms)
- 8 output enable product terms
- 1 synchronous preset term
- 1 asynchronous clear term

Figure 3. Logic Function Implementation in HY18CV8 Array



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Looking at the logic array diagram, the 36 input lines (0-35) run vertically and the 74 product terms (0-73) run horizontally. Each input line and product term intersection in the array has an associated programmable EEPROM memory cell that determines whether the intersection is connected or open. A connection allows an input line to become a logical input of the intersected product term (AND gate). Thus, each product term, although unlikely in a real application, truly equals a 36 input AND gate.

During programming of the HY18CV8, all EEPROM memory cells are first erased, opening all input line and product term intersections, specific intersections can then be selectively programmed for connection based on user defined logic functions. Figure 3 illustrates how a logic function, a 2 input exclusive NOR, is implemented in the HY18CV8 array. Note that if all true and complement inputs of product term are left open, the output of the AND gate will be a logical true (HIGH). If both true and complement of one or more inputs are connected to a product term, the output of the AND gate is forced to a logical false(LOW).

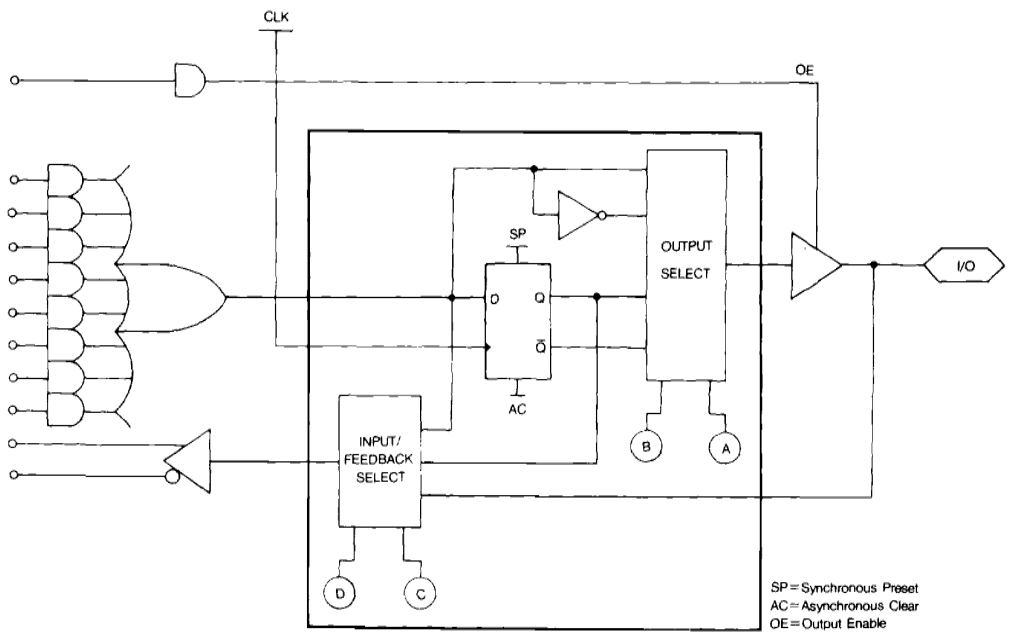
As illustrated in figure 2, the logic array has 64 product terms that are divided into groups of 8 each feeding into a sum (OR gate). By connecting specific inputs or I/O macro cell feedbacks to the product terms, complex sum-of-products logic functions can be created. Each sum feeds into its associated I/O macro cell where the logic function can be further controlled for output to an I/O pin of feedback into the array.

In addition to the 64 product terms of the 8 sum-of-product groups, there are 8 output enable product terms, 1 synchronous preset product term and 1 asynchronous clear product term. These additional terms are used to directly control specific I/O functions which are covered in the following section.

I/O MACRO CELL AND OUTPUT ENABLE OPERATION

A great amount of architectural flexibility is provided by the HY18CV8s reconfigurable I/O macro cells and independently controlled output endables. A closer look at the I/O macro

Figure 4. HY18CV8 Macro Cell Diagram



cell, figure 4, shows that it consists of a D-type flip-flop and two signal select multiplexers.

The D-type flip-flop operates similar to standard TTL D flip-flops to the extent that the D input is latched on the rising edge (LOW to HIGH transition) of the CLK input and Q or $\overline{Q}$ output signals can be used. Two additional inputs are controlled by the asynchronous clear and synchronous preset terms.

When the asynchronous clear product term is asserted (HIGH) the Q output will immediately be set to a LOW regardless of the clock state. When the synchronous preset term is asserted (HIGH) the Q output will be set to a HIGH on the following rising edge (LOW to HIGH transition) of the CLK input. Priority is given to the asynchronous clear signal if both asynchronous clear and synchronous preset have been asserted. Upon power-up, the asynchronous clear function is automatically performed setting the Q outputs of all macro cell flipflops to a LOW.

The two signal select multiplexers of each macro cell are controlled by four EEPROM programmable bits(A, B, C, and D) that determine which of the twelve possible configurations the macro cell will assume. This independent flexibility allows a single HY18CV8 to implement a combination of configurations among its eight macro cells. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The twelve possible I/O macro cell configurations are listed in Table 1, Their equivalent circuits are illustated in figure 5.

Each of the 8 output enable terms can enable or disable the output of its associated I/O macro cell. When the output enable product term is a logical true (HIGH) the output signal is enabled to the I/O pin. When it is a logical false (LOW) the I/O pin is in a high impedance state. The output enable product term allow individual I/O pins to be input only or bi-directional I/O.

DESIGN SECURITY

The HY18CV8 provides a special EEPROM security bit feature that prevents unauthorized reading or copying of designs implemented. The security bit feature is typically used after a design is finalized and ready for production. The actual setting of the security bit is done via the PLD programmer used. Once set, the verify (read) and program operation using a PLD programmer or other method will not be allowed until the entire device has first been erased.

CMOS EEPROM TECHNOLOGY

The performance and flexibility provided by the HY18CV8 is primarily due to HYUNDAI's advanced CMOS EEPROM technology offering low power, high speed and nonvolatile reprogrammability. Utilizing this technology along with special design techniques, the HY18CV8 maintains the low power characteristics of CMOS while achieving the speeds of standard bipolar PLDs.

For HY18CV8 reprogrammability, Fowler Nordheim tunneling techniques are employed to trap charges onto a floating gate through a thin oxide insulator. The trapped charges remain after power has been removed allowing nonvolatility of programmed data. The charges can be removed by electrically erasing the device. Once fully eraged, it can then be reprogrammed into a new configuration.

The HY18CV8 is designed for programming endurance of up to 1000 complete erase/reprogram cycles with a data retention of 10 years, when used within the specified operating temperature range. This means that the HY18CV8 can be reprogrammed up to 1000 times without degrading device operation, and similar to other non-volatile memory technologies, the data last programmed will remain valid for ten years.

Althought implemented in EEPROM technology, often associated with in-system reprogrammable memory devices, the HY18CV8 is

programmed out-of-system via a PLD programmer. There are several other beneficial reasons, however, for using EEPROM techonlogy. Some of these benefits include ; enhanced factory testing allowing 100% programming and functional integrity, cost effective "windowless" packaging and 3 second erase/reprogram time instead of approximately 20 minutes for EPROM PLDs.

Figure 5. HY18CV8 Macro Cell Configuration Equivalent Circuits

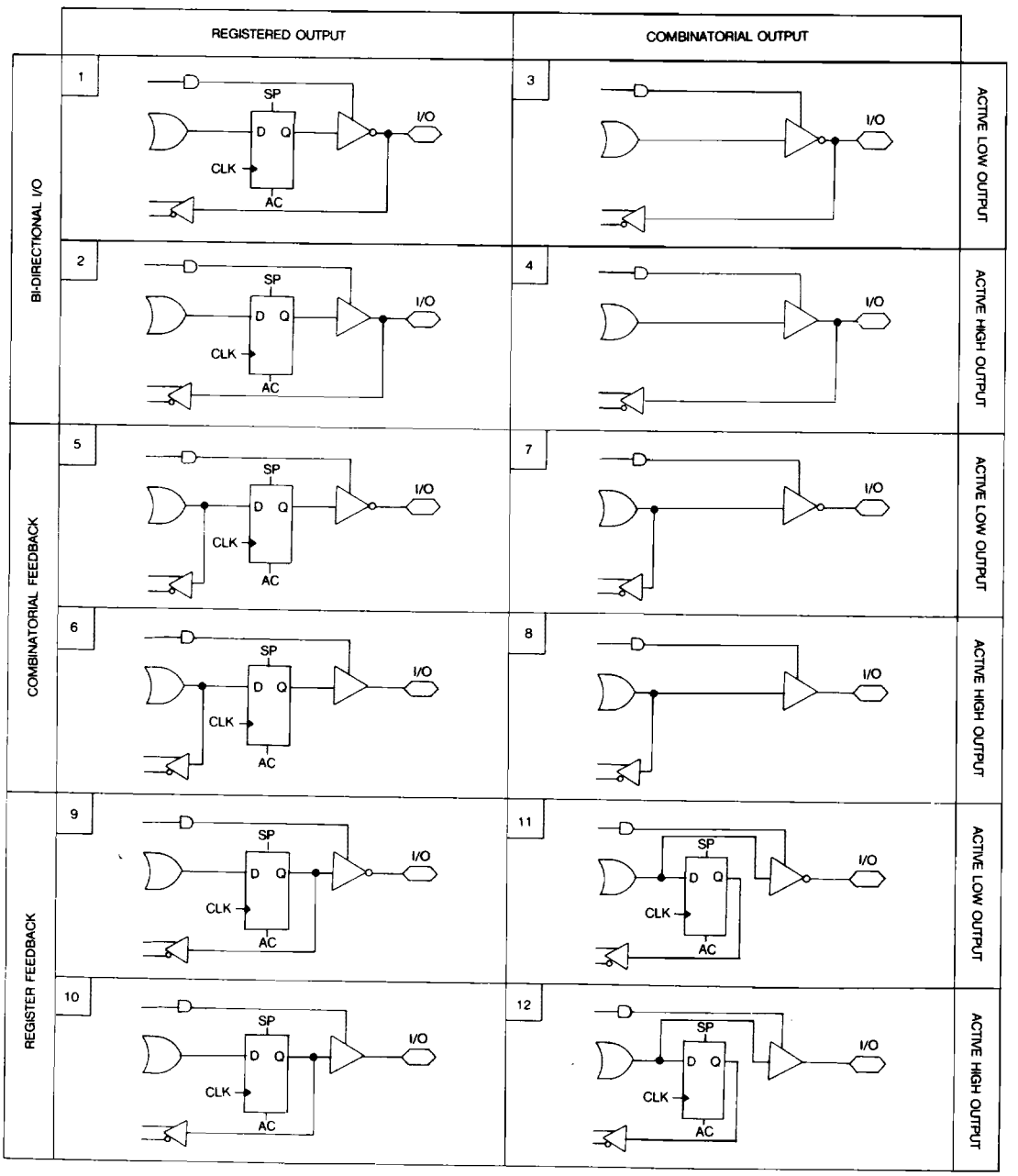


Table 1. HY18CV8 Macro Cell Configurations

CONFIGURATION					INPUT/FEEDBACK SELECT	OUTPUT SELECT	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Note : 0=programmed, 1=erased

APPLICATIONS OF THE HY18CV8

The versatility of the HY18CV8 makes it an effective alternative to conventional methods of logic design over a broad range of applications.

SSI/MSI logic replacement, the HY18CV8 enhances the design process with increased flexibility, higher performance, faster development time and design security. Manufacturing benefits are also realized by requiring fewer components and interconnects resulting in more efficient use of space, simplified inventory control and higher reliability.

As a bipolar PAL® replacement, the HY18CV8 has comparable speed and offers several advantages including : enhanced design flexibility, simplified inventory control, reduced power consumption, reprogrammability, and 100% factory testability for function and programming.

Design flexbility is of particular importance since the HY18CV8 not only emulates the majorty of the 20 pin PAL® devices (see table 2) but also allows functions found among several PAL® device types to be combined. In addition, completely new functions, not supported by the standard PAL® devices, can be implemented. This flexibility means a designer can focus on the design rather than on the restrictions of a fixed architecture. Reprogrammability is also a key benefit over one time programmable PAL®s. This feature adds convenience and cost savings in development prototyping and field retrofitting of systems. Converting existing PAL® designs to the HY18CV8 for plug-in replacement is easily accomplished using EEPLD evaluation or development tools.

As a design alternative to low-density gate arrays, one or more HY18CV8s offer a cost effective and low-risk option. With its architectural

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Table 2. 20 pin PAL® devices that can be emulated by the HY18CV8

OUTPUT TYPE	PART NUMBER AND I/O CAPACITY							
Combinatorial-High	10H8	12H6	14H4	16H2		16H8	16HD8	
Combinatorial-Low	10L8	12L6	14L4	16L2	16L8	16LD8		
Combinatorial-Polarity							16P8	18P8
Registered-Low					16R4	16R6	16R8	
Registered-Polarity					16RP4	16RP6	16RP8	

flexibility and equivalent gate density of approximately 300 gates, designs traditionally employing low-density gate arrays can be implemented quickly at no factory development (NRE) cost. Unlike the lead times encountered with gate arrays, the HY18CV8 is off-the-shelf available. Furthermore, if a design error is made or an upgrade is necessary, the changes can simply be reprogrammed.

Similar to SSI/MSI logic, PAL®s and low density gate arrays, applications of the HY18CV8 cover all the primary areas of system design including, data processing, communications, consumer, military and transportation. Specific functions implemented using the HY18CV8 range from basic logic and system support circuitry to stand alone controllers.
Some applications include :

- **SSI/MSI Logic Replacement/Customization**
  - Random logic
  - Decoders/encoders
  - Comparators
  - Multiplexers
  - Counters
  - Shift registers
- **Processor System Support**
  - Address decoding
  - Wait-state generation
  - Memory protection
  - Memory refresh
  - DMA control
  - Interrupt control
  - Timer/counter functions
  - Bus arbitation and interface
  - Error detection and correction
- **I/O Interface and Support**
  - Intelligent I/O port
  - Data communication interface
  - Display interface
  - Keyboard scanning
  - Disk and tape drive control
  - Front panel interface
- **Stand-Alone Non μP Based Controllers**
  - Motor control
  - Sensor monitoring
  - Security access control
  - Display control

ABSOLUTE MAXIMUM RATINGS[10]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply Voltage	Relative to GND	−0.5 to 7.0	V
V_I	Voltage Applied to Input[5]	Relative to GND[1]	−0.5 to 7.0	V
V_O	Voltage Applied to Output	Relative to GND[1]	−0.5 to 7.0	V
I_O	Output Current	Per Pin(I_{OL}, I_{OH})	± 25	mA
T_{ST}	Storage Temperature		−65 to 125	°C
T_{LT}	Lead Temperature	Soldering 10 second	300	°C

OPERATING RANGES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Operating Temperature	Commercial	0	70	°C
t_R	Clock Rise Time	See note 3		250	ns
t_F	Clock Fall Time	See note 3		250	ns
t_{RVCC}	V_{CC} Rise Time	See note 3		10	ms

DC ELECTRICAL CHARACTERISTICS

(Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC}=Min, I_{OH}=−4.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min, I_{OL}=8mA		0.45	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
$\lvert I_{IL} \rvert$	Input Leakage Current	V_{CC}=Max, GND≤V_{IN}≤V_{CC}		10	μA
$\lvert I_{OZ} \rvert$	Output Leakage Current	I/O=High-Z, GND≤V_O≤V_{CC}		10	μA
I_{SC}	Output Short Circuit Current	V_{CC}=Max, V_O=0.5V[9]	−30	−100	mA
I_{CCSC}	V_{CC} Current, Active, CMOS	V_{IN}=V_{CC} or GND[4]		20	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN}=V_{CC} or GND[4] All outputs open[4]		I_{CCSC}+ 0.7mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN}=V_{IL} or V_{IH}[4]		25	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN}=V_{IL} or V_{IH}, All outputs open[4]		I_{CCST}+ 0.7mA/MHz	mA

CAPACITANCE[7]

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	T_A=25°C, f=1MHz, V_{CC}=5.0V		6	pF
C_{OUT}	Output Capacitance	T_A=25°C, f=1MHz, V_{CC}=5.0V		12	pF

AC ELECTRICAL CHARACTERISTICS[2]

(Over Operating Range)

SYMBOL	PARAMETER	HY18CV8-25		HY18CV8-30		HY18CV8-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PD}	Input[5] or feedback to non-registered output		25		30		35	ns
t_{OE}	Input[6] to output enable		25		30		35	ns
t_{OD}	Input[6] to output disable		25		30		35	ns
t_{CO1}	Clock to output		18		20		22	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35		45		50	ns
t_{SC}	Input[5] or feedback setup to clock	20		25		30		ns
t_{HC}	Input[5] hold after clock	0		0		0		ns
t_{CL}, t_{CH}	Clock width-CLK low time, CLK high time[3]	15		15		15		ns
t_{CP1}	Clock period (register feedback to registered output via internal path)	30		40		45		ns
t_{MAX1}	Maximum clock frequency($1/t_{CP1}$)		33.3		25		22.2	MHz
t_{CP2}	Clock period(t_{SC}+t_{CO1})	35		45		50		ns
t_{MAX2}	Maximum clock frequency($1/t_{CP2}$)		28.5		22.2		20	MHz
t_{AW}	Asynchronous clear pulse width	25		30		35		ns
t_{AP}	Input[5] to asynchronous clear		30		35		40	ns
t_{AR}	Asynchronous reset recovery time		20		25		30	ns
t_{RESET}	Power-on reset time for register in clear state.[3]		5		5		5	μs

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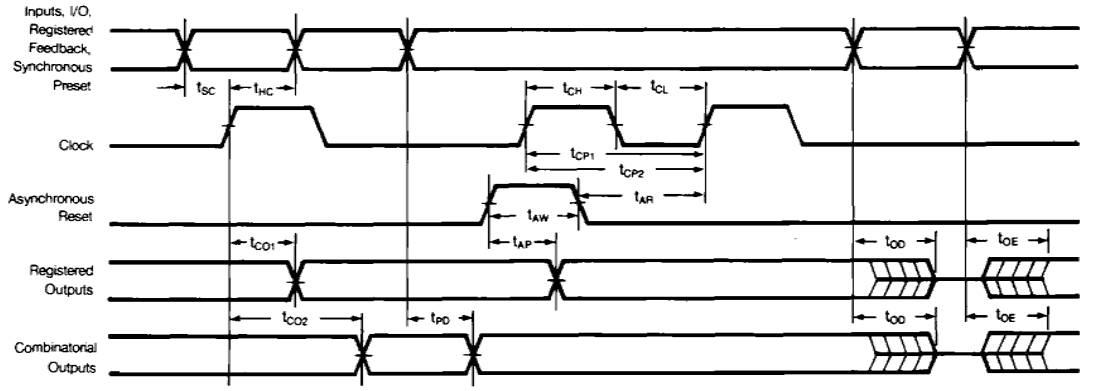
SWITCHING WAVEFORMS

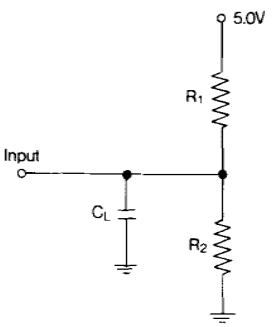


NOTES

1. Minimum DC input is −0.5V, however inputs may undershoot to −2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are open (no load).
5. "Input" refers to input pin signal.
6. t_{OE} is measured from input transition to $V_{REF}\pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V ; V_{REF}=1.90V for TTL interface for 2.375V for CMOS interface.
7. Capacitances are tested on a sample basis.
8. Test conditions assume : signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration less than 1 second.
10. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

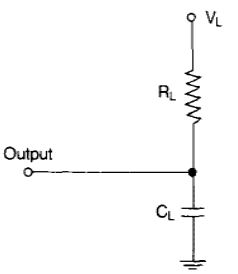
AC EQUIVALENT LOAD CIRCUIT

TEST LOAD



CMOS INTERFACE	TTL INTERFACE
R_1=480KΩ	R_1=464Ω
R_2=480KΩ	R_2=250Ω
C_L=30pF	C_L=30pF

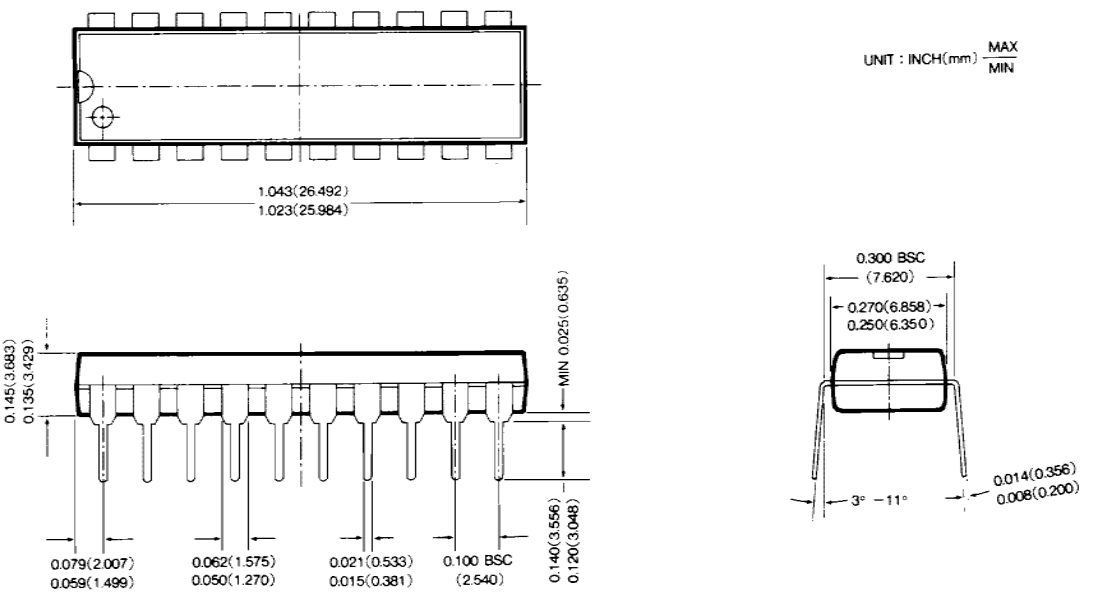
THEVENIN



CMOS INTERFACE	TTL INTERFACE
R_L=228KΩ	R_L=163Ω
V_L=2.375V	V_L=1.75V
C_L=30pF	C_L=30pF

PACKAGE INFORMATION

- **20 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL**



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MEMO